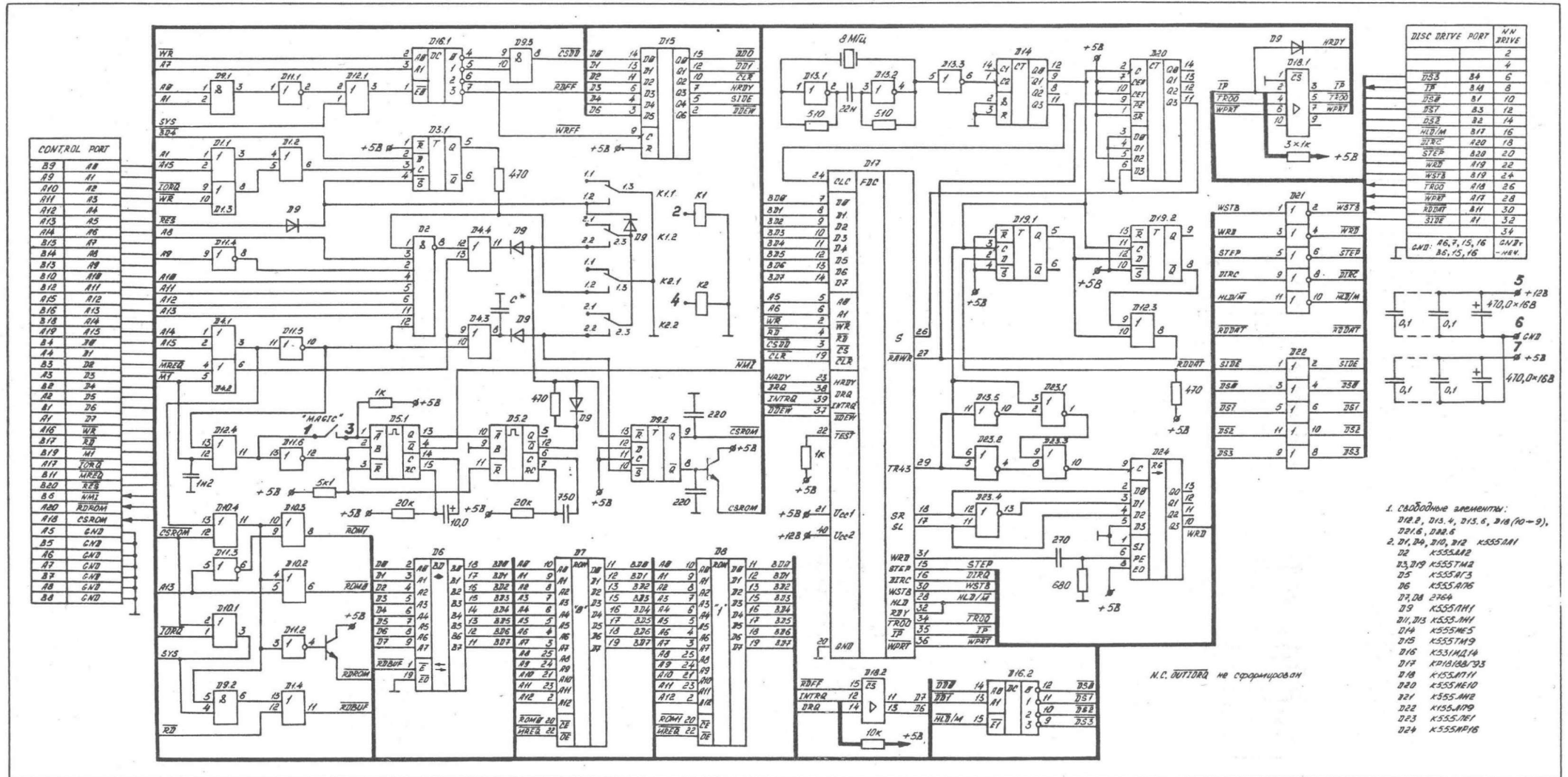
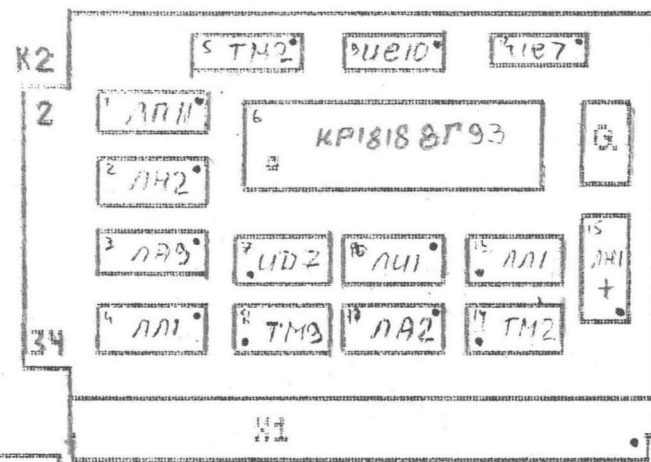
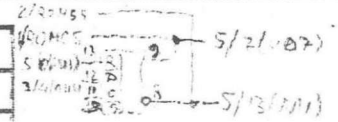


BETADISC INTERFACE 1



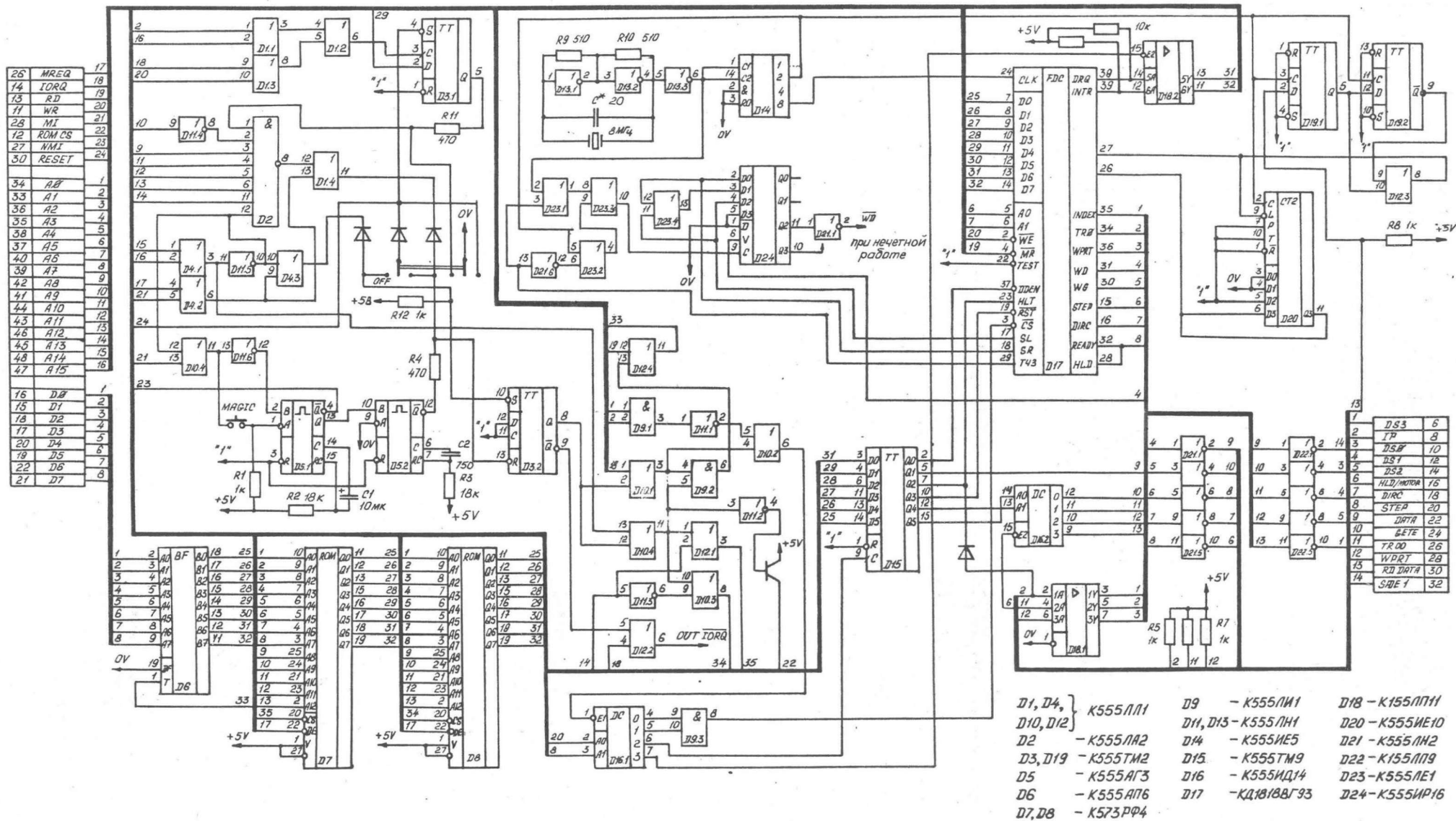


K2	20-STEP
	18-OTAC
	16-START
	24-WR
	22-UD
	32-SIDE
	26-TR00
	10-SEL A
	12-SEL B
	8-ID
	28-WPRT
	30-ROOT

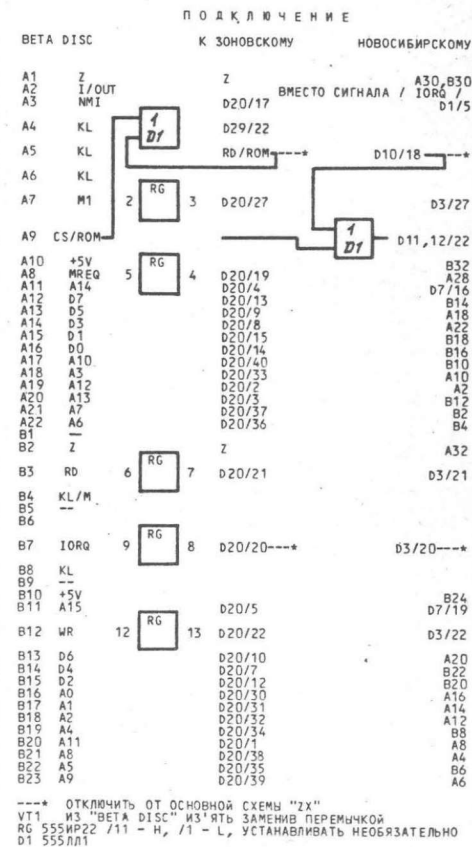
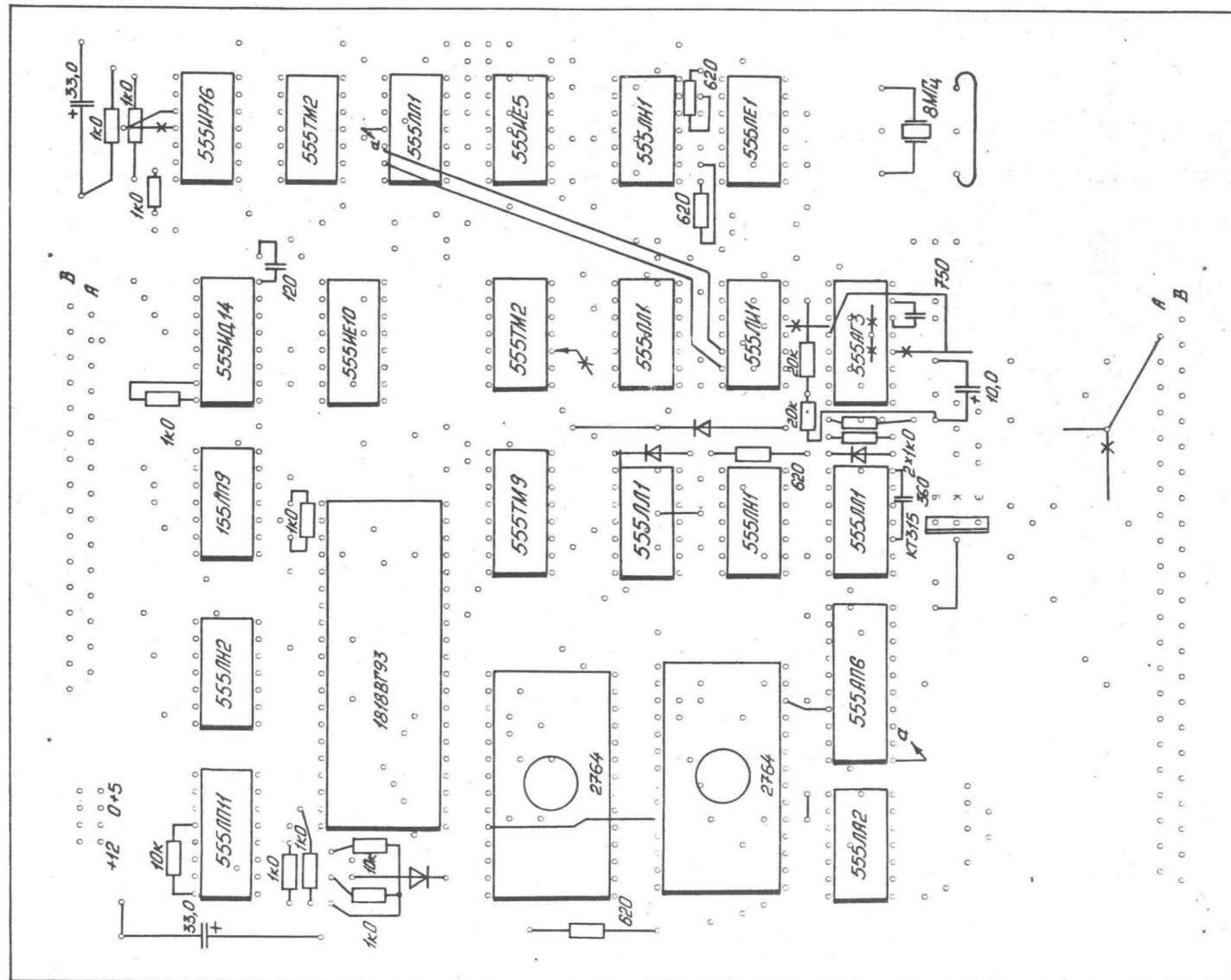


A1 - ROMCS	+	A20 - D4	-	B1 - OUT IRQ	+	B19 - D0	+
A2 - ROMCS	+	A21 - D3	+	B7 - +5V	-	B20 - D1	+
A7 - +5V	+	A22 - OEWL	+	B10 - A12	-	B21 - D2	+
A10 - A13	+	A23 - OEWL	+	B11 - A7	-	B22 - OEWL	+
A11 - A8	+	A25 - M1 up22	+	B12 - A6	-	B24 - RESET	+
A12 - A9	+	A26 - WR up22	+	B13 - A5	-	B27 - RD up22	+
A13 - A11	+	A27 - IORQ up22	+	B14 - A4	+	B28 - MREQ up22	+
A15 - A10	+	A28 - NMI	+	B15 - A3	+	B30 - A15	+
A17 - D7	+	A30 - A14	+	B16 - A2	+	B32 - +12V	+
A18 - D6	+	A32 - +12V	+	B17 - A1	+		
A19 - D5	+			B18 - A0	+		

BETADISC INTERFACE 0

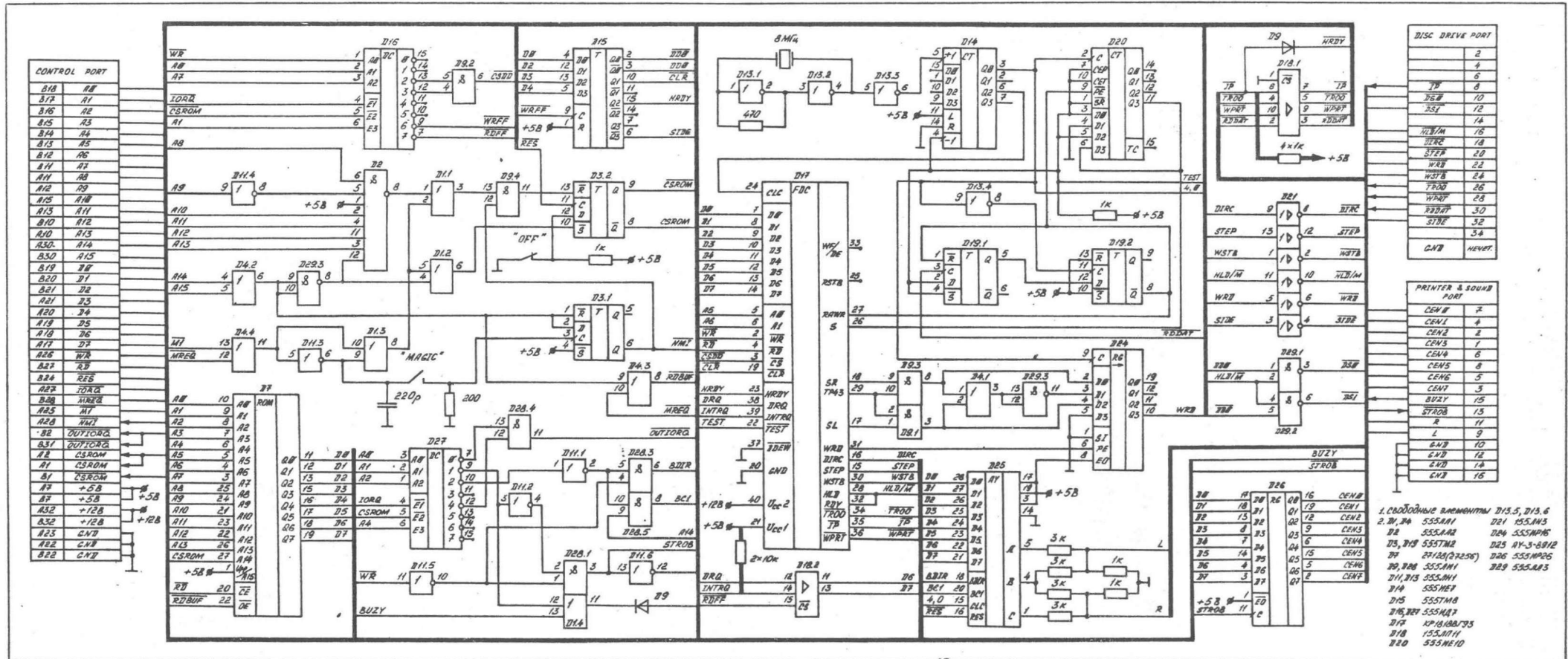


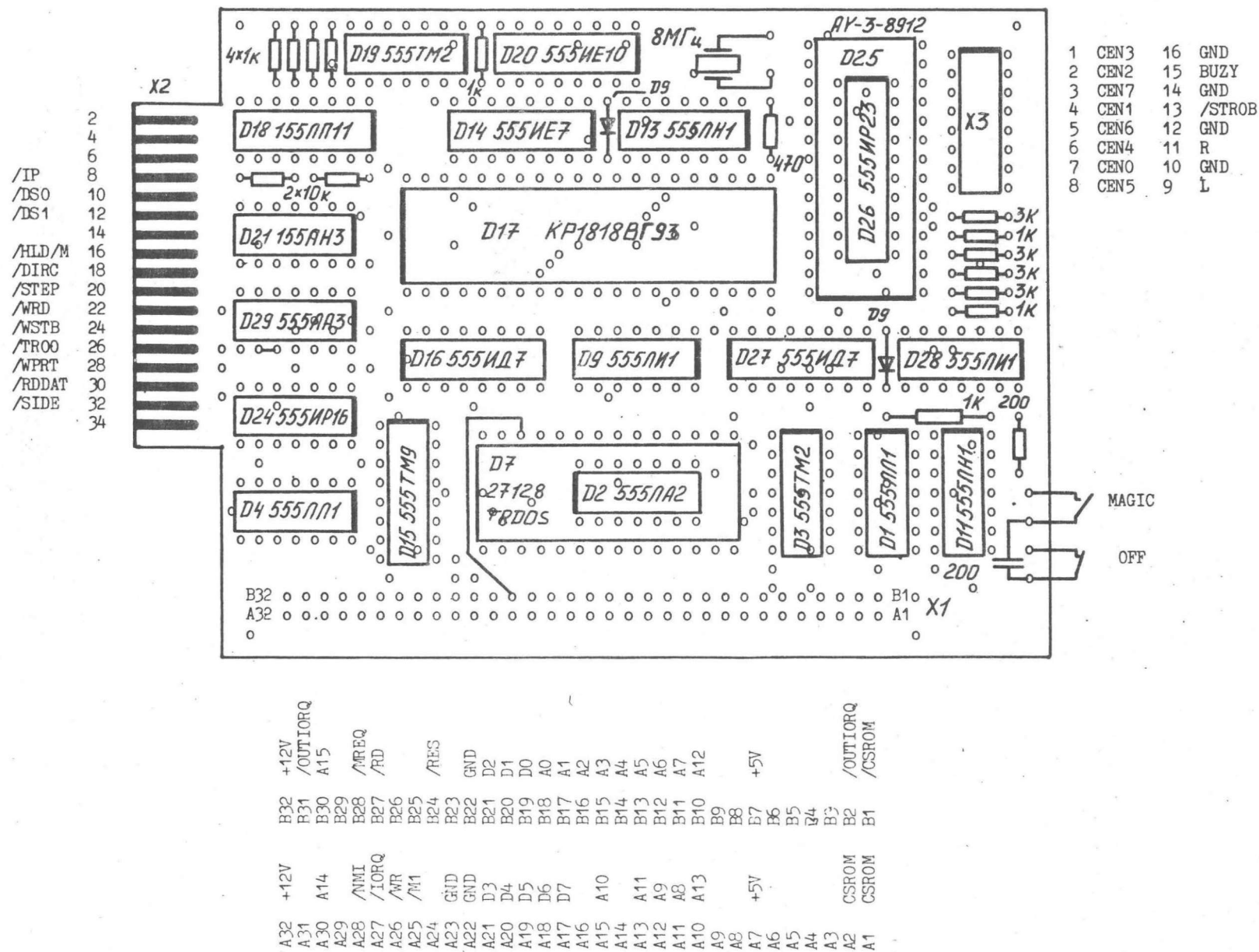
A11 DS3 6
 A2 IP 8
 A10 ASD 10
 A12 DS4 12
 A13 DS2 14
 A14 HLD/M 16
 A8 DIRC 18
 A7 STEP 20
 A5 WR/DAT 22
 A6 GETE 24
 A3 TR00 26
 A4 WPRT 28
 A15 RD/DAT 30
 A9 SIDE 1 32
 A1 +12V
 B1 2 +5V
 B3, 4, 15, 16 Z





BETADISC INTERFASE 2

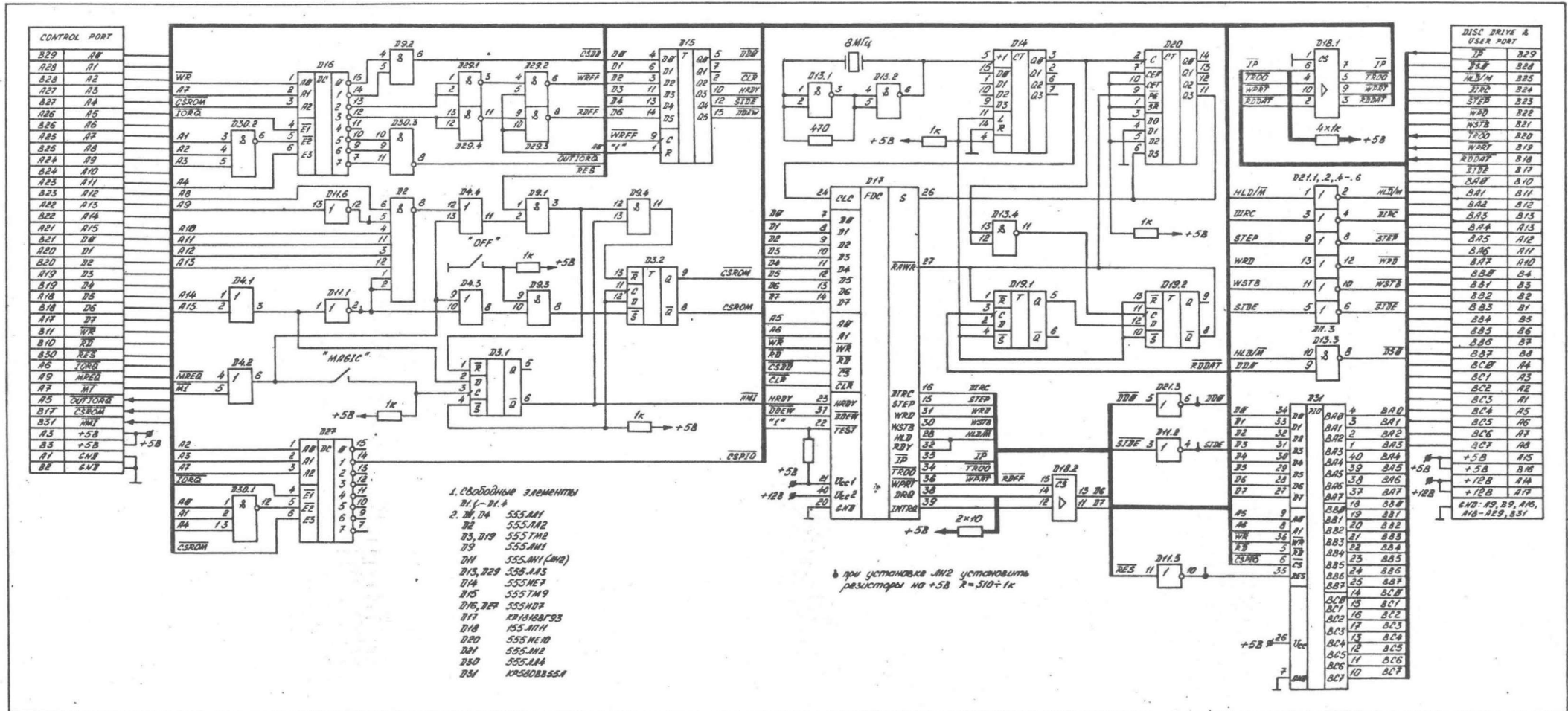




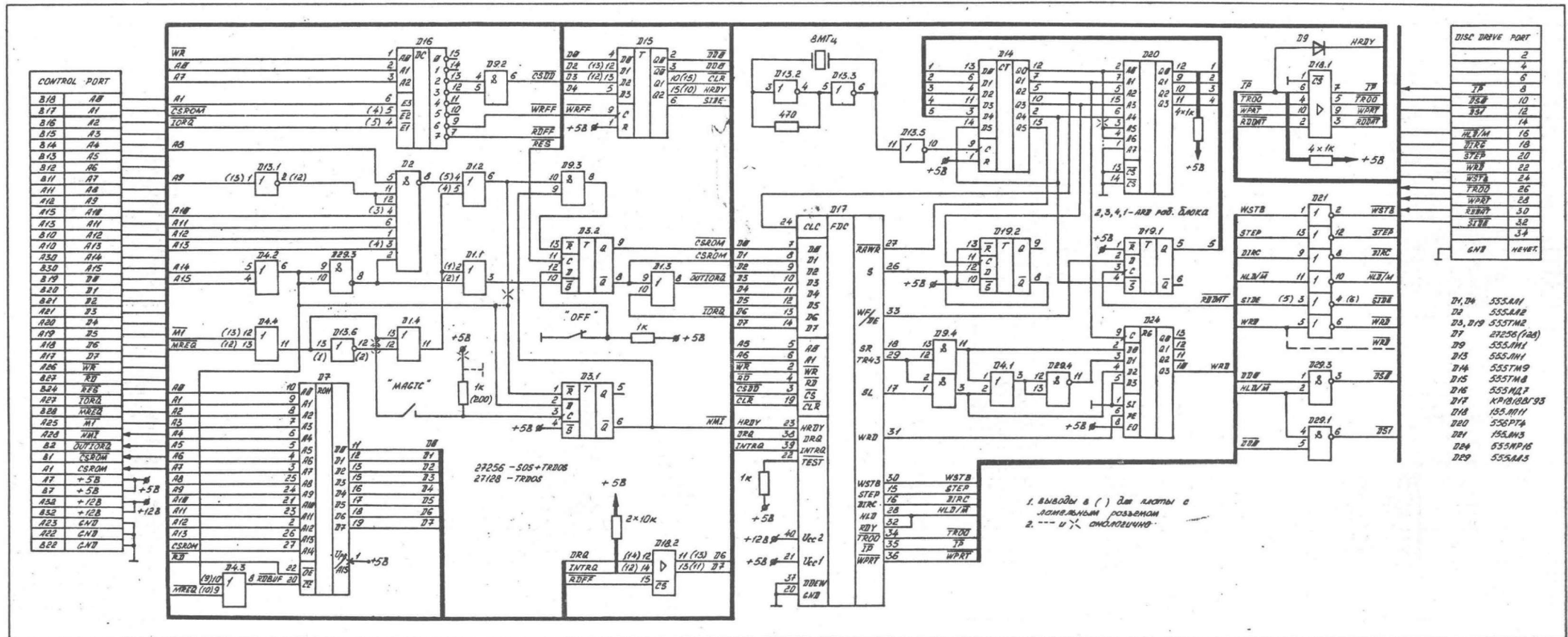
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BETADISC INTERFASE 3

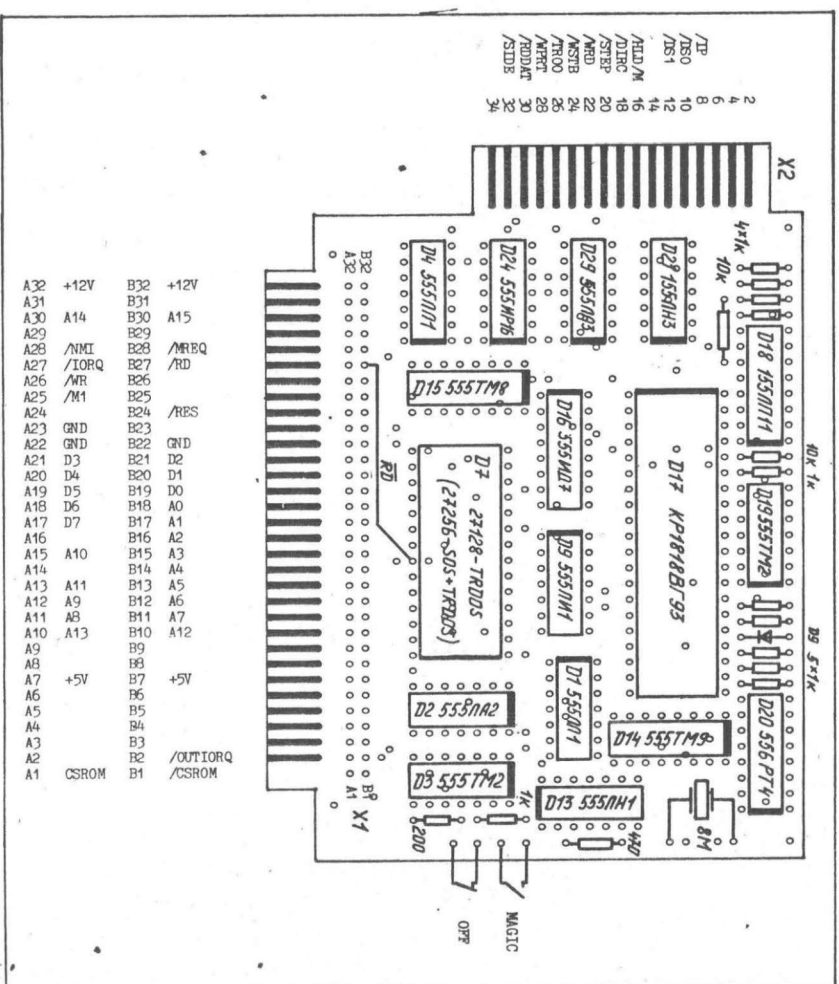
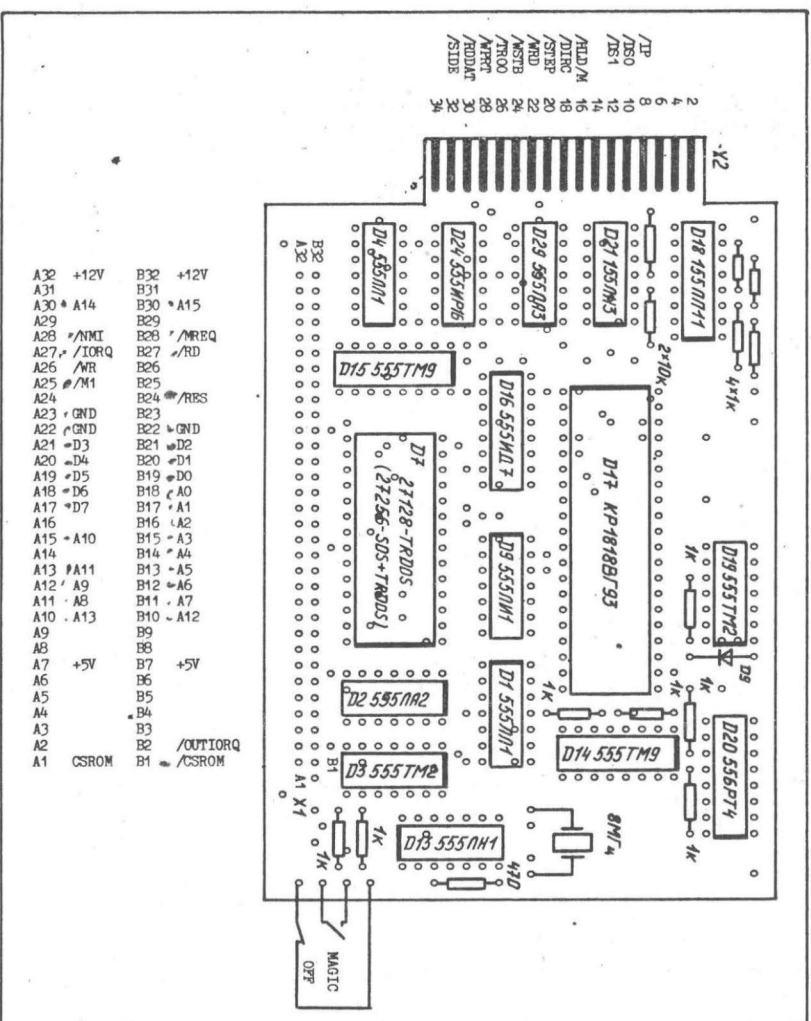


BETADISC INTERFACE 4

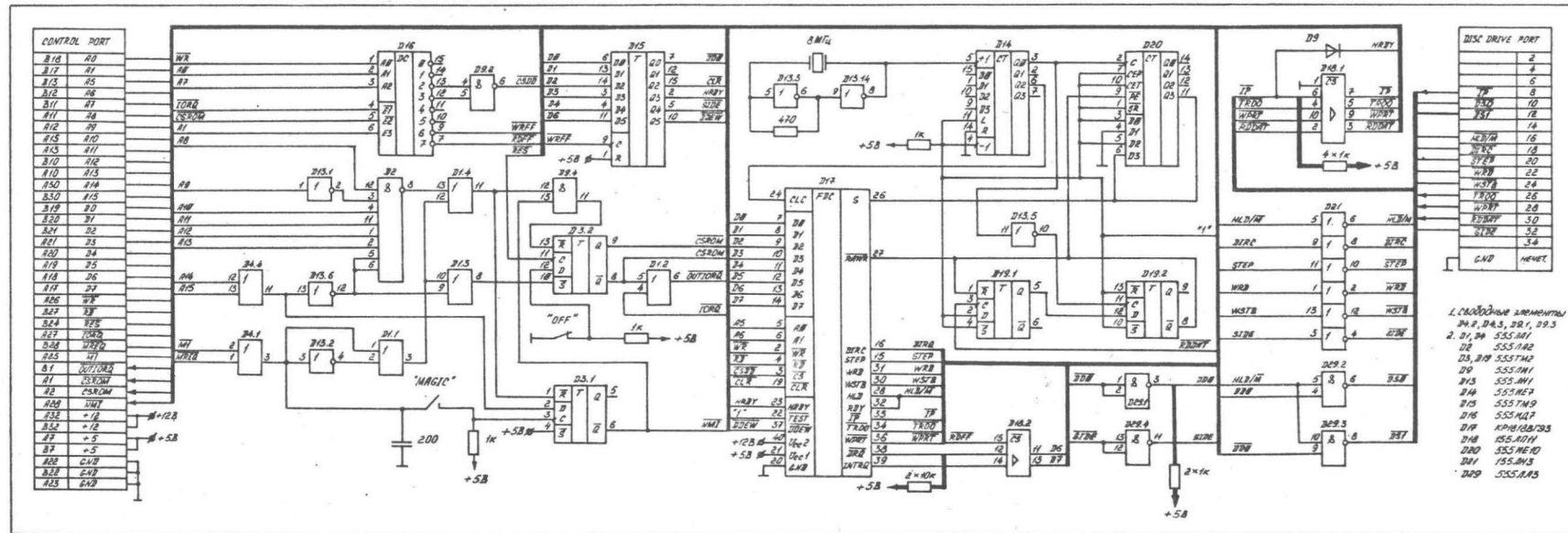


BETADISC INTERFACE 4

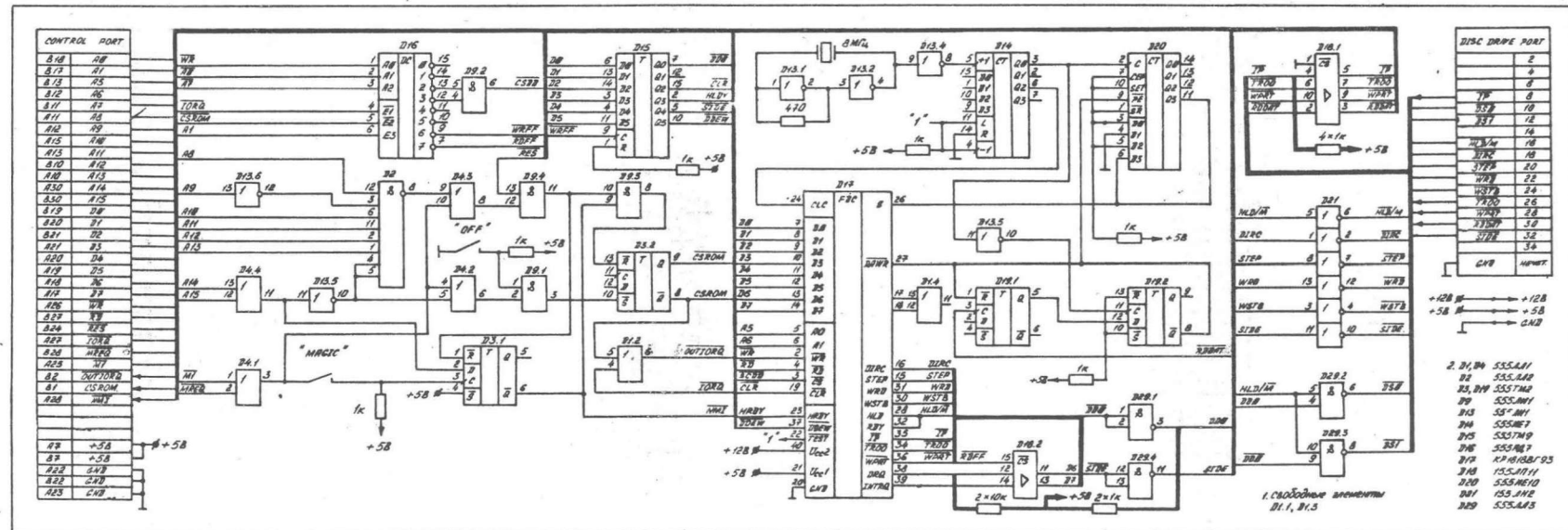
BETADISC INTERFACE 4



BETADISC INTERFAS 5

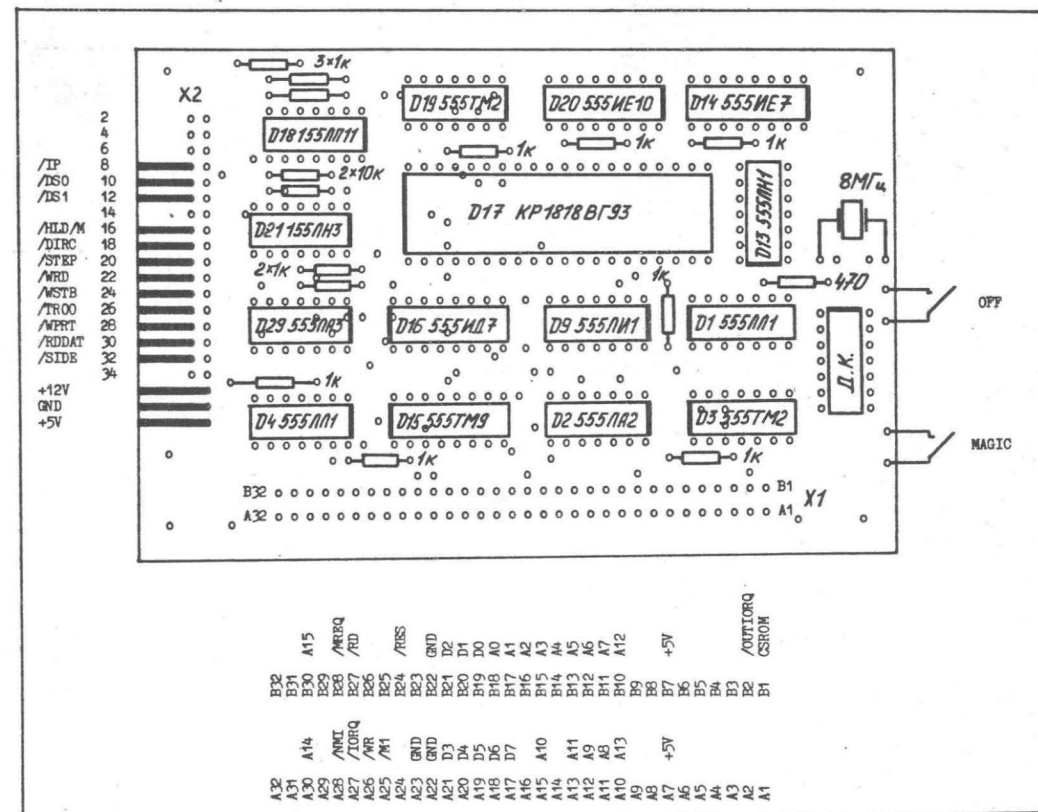
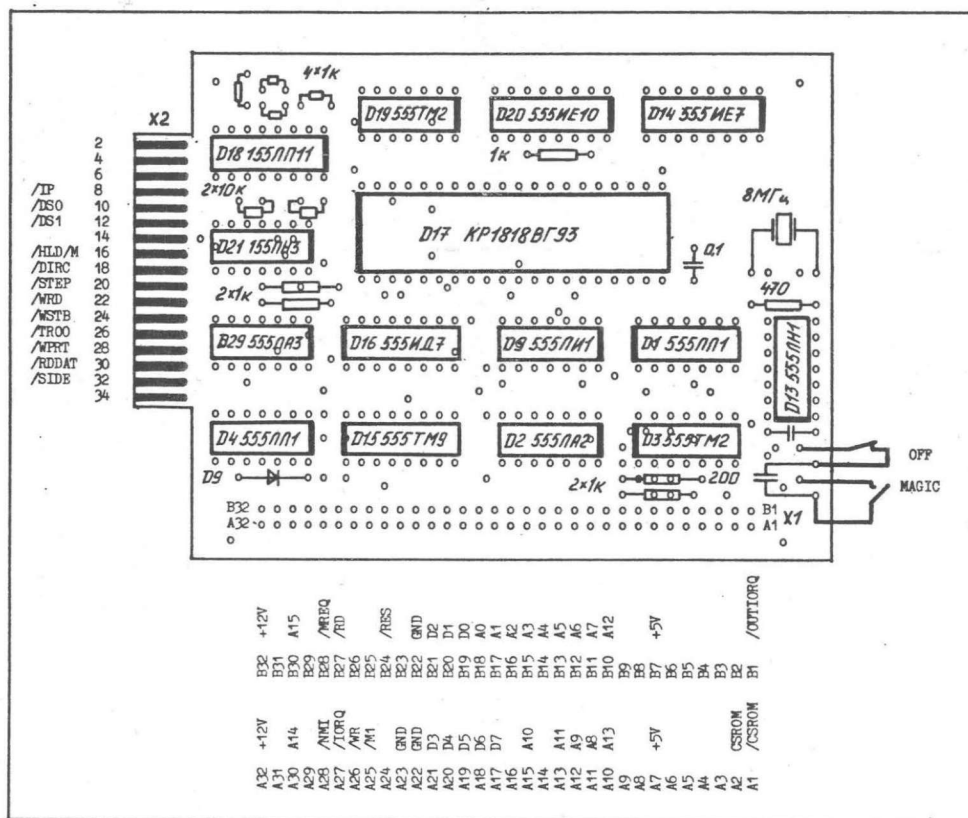


BETADISC INTERFAS 6



BETADISC INTERFASE 5

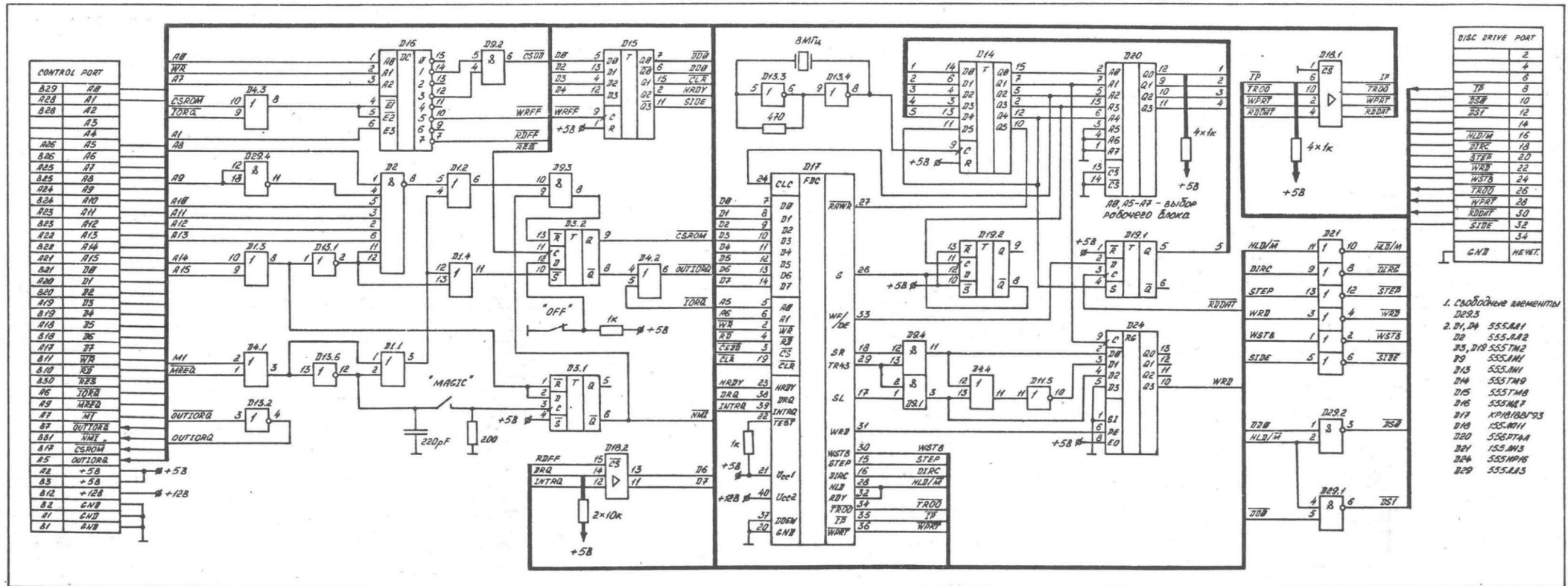
BETADISC INTERFASE 6



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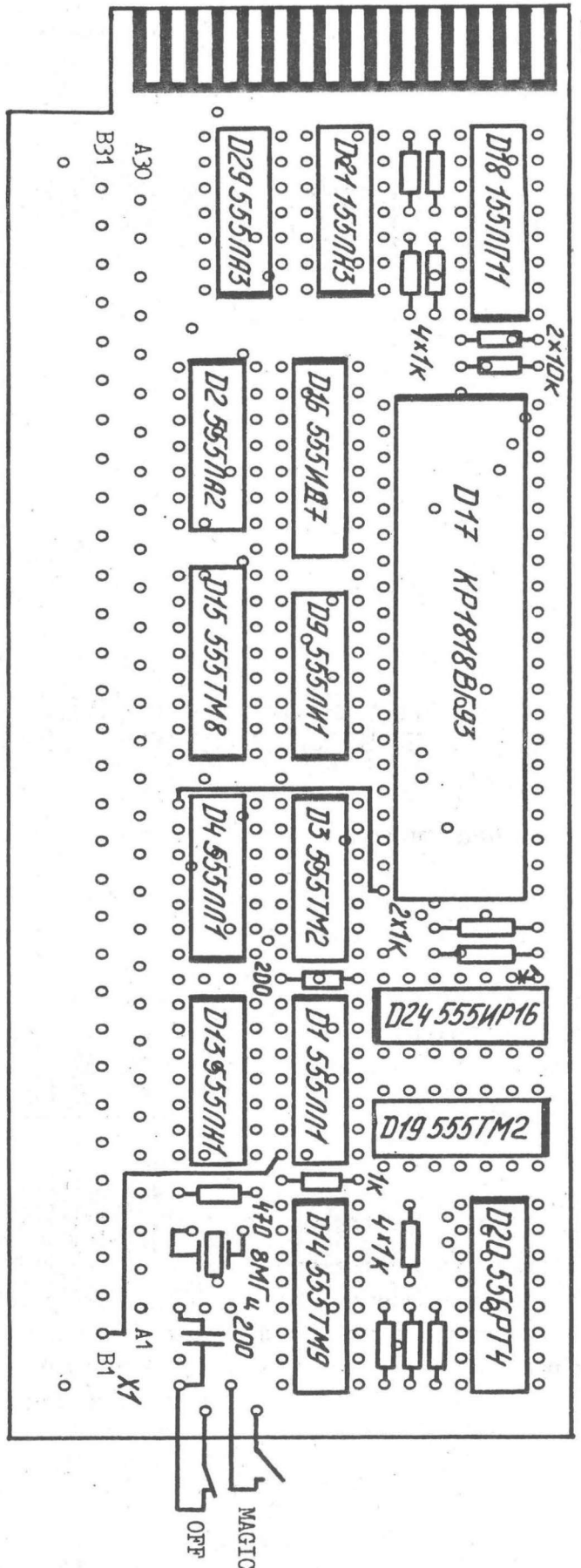
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BETADISC INTERFASE 7



X2

34 /SIDE
32 /RDATA
30 /WPRT
28 /PROO
26 /MSTB
24 /WRD
22 /STEP
20 /DIRC
18 /HLD/M
16 /DS1
14 /DS0
12 /IP
10
8
6
4
2



A30	B31	/NMI
A29	B30	/RES
A28 A1	B29	A0
A27	B28	A2
A26 A5	B27	A6
A25	B26	A8
A24	B25	A10
A23 A11	B24	A12
A22 A13	B23	A14
A21 A15	B22	D0
A20 D1	B21	D2
A19 D3	B20	D4
A18 D5	B19	D6
A17 D7	B18	/CSROM
A16	B17	
A15	B16	
A14	B15	
A13	B14	
A12	B13	
A11	B12	+12V
A10	B11	/WR
A9 /MREQ	B10	/RD
A8	B9	
A7 /M1	B8	
A6 /IORQ	B7	/OUTIORQ
A5 OUTIORQ	B6	
A4	B5	
A3	B4	
A2 +5V	B3	+5V
A1 GND	B2	GND
	B1	GND

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BETA DISK

